

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Kwan-Yong LIM, et al.

Serial No.: New Application Group Art Unit: Not Yet Assigned

Filed: July 10, 2003 Examiner: Not Yet Assigned

Title: STACK GATE ELECTRODE SUPPRESSED WITH INTERFACE-REACTION  
AND METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING THE  
SAME

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

July 10, 2003

Sir:

As a means of complying with the duty of disclosure under 37 CFR §1.56, and in accordance with 37 CFR §§1.97 and 1.98, Applicant(s), through the undersigned attorney, submits this Information Disclosure Statement. The patents, publications or other information submitted herewith are listed on the attached Form PTO-1449 and copies are attached.

In accordance with 37 CFR §1.97(b)(1) or (2), this Information Disclosure Statement is being filed either within three months of the filing date of the above-identified application, or within three months of the date of entry into the national stage of the above-identified application as set forth in 37 CFR §1.491. Accordingly, no fee is required.

Respectfully submitted,

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## LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.: P68987US0 GROUP ART UNIT: Not Yet Assigned  
 SERIAL NO.: Not Yet Assigned FILING DATE: July 10, 2003  
 APPLICANT(S): Kwan-Yong LIM, et al. TODAY'S DATE: July 10, 2003

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## U.S. PATENT DOCUMENTS

*EXAMINER <u>██████████</u>	DOCUMENT NUMBER	DATE	NAME	INT'L CLASS	SUB- CLASS	FILING DATE (If Appropriate)
<u>██████████</u>	<u>AA 5,719,410</u>	<u>2/17/98</u>	<u>Suehiro, et al.</u>	<u>H01L</u>	<u>23/48</u>	<u>12/16/96</u>
<u>██████████</u>	<u>AB 6,100,193</u>	<u>8/08/00</u>	<u>Suehiro, et al.</u>	<u>H01L</u>	<u>21/44</u>	<u>09/24/97</u>
<u>██████████</u>	<u>AC</u>	<u>██████████</u>	<u>██████████</u>	<u>██████████</u>	<u>██████████</u>	<u>██████████</u>

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## FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	SUB- CLASS	TRANSLATION (YES) (NO)
<u>██████████</u>	<u>AD</u>	<u>██████████</u>	<u>██████████</u>	<u>██████████</u>
<u>██████████</u>	<u>AE</u>	<u>██████████</u>	<u>██████████</u>	<u>██████████</u>

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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

<u>██████████</u>	<u>AF</u>	<u>██████████</u>
<u>██████████</u>	<u>AG</u>	<u>██████████</u>

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EXAMINER Paula Colodner DATE CONSIDERED 12/1/2003

\* EXAMINER? Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

## **Information Disclosure Statement**

New U.S. Patent Application for  
STACK GATE ELECTRODE SUPPRESSED WITH INTERFACE-REACTION  
AND METHOD FOR FABRICATING SEMICONDUCTOR DEVICE  
HAVING THE SAME  
Our Ref. No.: P02HA065/US/cj

Reference No.:

- (1) US Patent No. 5,719,410
- (2) US Patent No. 6,100,193